REMARKS

The Examiner is thanked for the continued indication that claims 3 and 14 define allowable subject matter. The FINAL Office Action, however, has advanced the same rejections as those advanced in the previous, non-Final Office Action. In response, Applicants submit these amendments to address the rejections under 35 U.S.C. §112, second paragraph, to place the claims of this application in better condition for appeal.

Discussion of Rejections Under 35 U.S.C. § 112, Second Paragraph

The Office Action rejected all claims under 35 U.S.C. § 112, second paragraph for various, stated reasons. Applicants respectfully submit that, in view of the above amendments and following remarks, that each of these rejections should be withdrawn. In this regard, independent claims 1, 11, and 20 have each been amended to specify, among other things, that

the "portion of the system bus comprises a plurality of signal of signal lines of the system bus, but not all of the signal lines of the system bus."

The Office Action then rejected all claims under 35 U.S.C. § 112, second paragraph, alleging that "essential structure cooperative relationships between elements in the claims ... have been omitted." In support of this rejection, the Office Action cites MPEP 2172.01 (Unclaimed Essential Subject Matter), and states that "MPEP 2172.01 requires that relationships between elements recited in claims must be specified." This reflects a misunderstanding of MPEP 2172.01. In fact, MPEP 2172.01 specifically states:

> ... *Ex parte Nolden*, 149 U.S.P.Q. 378, 380 (Bd. Pat. App. 1965)("It is not essential to a patentable combination that there be

> interdependency between the elements of the claimed device or that all the elements operate concurrently toward the desired result"); *Ex parte Huber*, 148 U.S.P.Q. 447, 448-449 (Bd. Pat. App. 1965) (A claim does not necessarily fail to comply with 35 U.S.C. 112, second paragraph where the various elements do not function simultaneously, are not directly functionally related, do not directly intercooperate, and/or serve independent purposes.

Thus, MPEP 2172 states just the opposite of what the Office Action appears to allege.

Pursuant to the invitation set out at the bottom of page 3 and top of page 4 of the Office Action (underlined), Applicants hereby note their disagreement with the position taken by the Office Action, and submit that the claims, as filed, recited all necessary or essential interrelationships between the elements. In this regard, Applicants note that each claim element makes appropriate relational reference to other claim elements, such that no element is in isolation and therefore appropriate and proper structural interrelationships among claim elements are properly provided. In addition, the Examiner stated that the claims are indefinite because they allegedly do not recite the required structural interrelationship of "essential elements to the claimed invention." The MPEP, however, does not define what is an "essential" element, nor did the Examiner provide a definition of what constitutes an "essential" element.

Further, and despite Applicants' invitation in the previous response, the Examiner did not set forth any explanation or illustration of why the claims allegedly failed to satisfy MPEP 2172, or what exemplary language could have been added to bring the claims into conformity. The Examiner apparently had a good working understanding of the claims (as is required by MPEP 904 before initiating a search, and as reflected in the application of prior art as allegedly anticipating the claims). Accordingly, Applicants respectfully request the Examiner to provide more helpful

insight into this rejection (either by more fully stating the rejection or by providing exemplary language that would overcome the rejection), should the Examiner disagree with Applicants' position and maintain this rejection. In reconsidering this rejection, however, Applicants remind the Examiner that claim breadth should not be confused with indefiniteness (see MPEP 2173.04).

In view of the foregoing, Applicants respectfully submit that all claims, as amended, fully comply with the requirements of 35 U.S.C. § 112, second paragraph, and Applicants respectfully request that the rejections thereof be reconsidered and withdrawn.

Discussion of Rejections Under 35 U.S.C. § 102

On a substantive basis, the Office Action rejected the independent claims (claims 1, 11, and 20) under 35 U.S.C. § 102 as allegedly anticipated by U.S. Patent 6,172,906 (hereafter the '906 patent). For at least the reasons set forth herein, Applicants respectfully request reconsideration of the rejection.

With regard to claim 1, claim 1 recites:

> 1. An integrated circuit component comprising:
> logic capable of being configured to interface with a first portion of a system bus, wherein the first portion of the system bus comprises a first plurality of signal lines of the system bus, but not all of the signal lines of the system bus; and
> ***logic capable of being configured to interface with a companion integrated circuit and to receive information that is communicated from the companion integrated circuit, which information was communicated to the companion integrated circuit via a second portion of the system bus wherein the second portion of the signal bus comprises a second plurality of signal***

lines of the system bus, which are not a part of the first plurality of signal lines.

(*Emphasis added*). Applicants respectfully submit that claim 1 patently defines over the '906 patent for at least the reasons that the '906 patent fails to disclose the features emphasized above.

Notably, claim 1 is directed to "an integrated circuit component" (i.e., a single component) that includes two separate logic blocks. A first logic block is capable of being configured to interface with a first portion of a system bus. Likewise, the second logic block is capable of being configured to interface with a companion integrated circuit and to receive information that is communicated from the companion integrated circuit, which information was communicated to the companion integrated circuit via a second portion of the system bus. Simply stated, these features are not disclosed in the '906 patent.

To assist the Examiner in a better understanding of claim 1, consider the embodiment of Fig. 2 of the present application. The integrated circuit corresponds to reference numeral 210, while the companion integrated circuit corresponds to reference numeral 211. The first-recited logic element corresponds to split bus logic 214 of integrated circuit 210, while the second-recited logic element corresponds to split bus logic 215 of integrated circuit 210. As is illustrated in Fig. 2, and more particularly claimed in claim 1, the first-recited logic element (e.g., split bus logic 214) is capable of being configured to interface with a first portion of the system bus 105. Likewise, the second-recited logic (e.g., split bus logic 215) is configured to communicate and receive information that is communicated over a second portion of a system bus and routed

through the companion integrated circuit 211. Similarly, claim 1 also covers the embodiment of Fig. 5.

The teachings applied by the Office Action from the '906 patent (disclosing two memory chips 670 and 672 of a memory bank 506) are simply inapplicable to the embodiments defined by claim 1. In this regard, the two memory chips 670 and 672 of the '906 patent are separate integrated circuits, and not a single integrated circuit as required by claim 1.

The FINAL Office Action responded to this previous argument by citing FIGs. 1 and 6. It appears that the Examiner is treating the reference number 600 (of the '906 patent) in FIG. 6, for example, as denoting a chip. However, it instead denotes an entire memory system. The specification of the '906 patent confirms this (see col. 6, line 36 and col. 7, lines 47-52). Indeed, the FINAL Office Action (p. 15) states:

> Contrary to Applicants' argument, it is clear from at least Fig. 6a of Estakhri that the first companion integrated circuit (18/670) and the second companion integrated circuit (20/672) each is disposed in a single integrated circuit chip.

This position reflects at least one fundamental misapplication of Estakhri to claim 1. As set forth above, reference number 600 (of Fig. 6a) denotes a "memory system" (col. 6, line 36), and not a single integrated circuit. Reference number 506 denotes a "memory bank" (col. 6, line 57), and not a single integrated circuit. Finally, by the Examiner's own admission that reference number 670 comprises a first integrated circuit and reference number 672 comprises a second integrated circuit, the two separate integrated circuits cannot properly/logically comprise a single integrated circuit chip, as expressly claimed by claim 1.

Simply stated, there is no teaching in the '906 patent of a single integrated circuit having logic for interfacing with a first portion of a system bus (the first portion being less than all of the system bus) and second logic for interfacing with a companion integrated circuit to receive information communicated over a second portion of the system bus. As claims 2-10 depend from claim 1, the substantive rejections of those claims should be withdrawn for at least the same reasons.

With regard to independent claim 11, claim 11 recites:

> 11. A system comprising:
> a plurality of companion integrated circuit components that collectively implement a logic function embodied in a single, conventional integrated circuit component, ***each companion integrated circuit component comprising***:
> a first logic interface for communicating with a remote component via ***a portion of a system bus, wherein the portion of the system bus comprises a plurality of signal of signal lines of the system bus, but not all of the signal lines of the system bus***;
> ***a second logic interface for communication with a companion logic interface of a remaining one of the plurality of the integrated circuit components over a separate bus***; and
> logic for controlling the selective communication of information received by the first logic interface via the portion of the system bus through the second logic interface to the companion integrated circuit.

(*Emphasis added*). Applicants respectfully submit that claim 11 defines over the '906 patent for at least the reasons that the '906 patent fails to teach those features emphasized above.

Like the rejection of claim 1, the Office Action cites memory chips 670 and 672 as comprising the claimed "integrated circuit." It then cites register 671 as comprising the claimed first logic interface. Then, the Office Action cites the same register 671 as

comprising the claimed second logic interface. This rejection simply makes no sense, in the context of the claimed embodiments.

In this regard, the first logic interface is specifically claimed as "communicating with a remote component via a portion of a system bus." In contrast, the second logic interface is specifically claimed as being configured for "communication with companion logic interfaces of the remaining of the plurality of the integrated circuit components over a separate bus." This is not taught or disclosed in the '906 patent. In fact, the only input to the applied I/O register 671 is bit positions D[0:7] of the data bus 680. These bit positions couple to I/O register 671 at reference number 682. Significantly, the register 671 cannot comprise the claimed second logic interface, assuming that that register 671 comprises the first logic interface. Furthermore, the I/O registers 671 and 673 are disposed in separate integrated circuit chips, so these elements cannot be mixed and matched as applying to the first and second logic interfaces, as claim 11 requires that the first and second logic interfaces be in a single integrated circuit component.

For at least these reasons, the rejections of claim 11 should be withdrawn.

With regard to claim 20, independent claim 20 recites:

> 20. An integrated circuit component comprising:
> a first set of conductive pins for channeling communications with a remote component via only a portion of a system bus, wherein the portion of the system bus comprises a plurality of signal of signal lines of the system bus, but not all of the signal lines of the system bus;
> a second set of conductive pins for channeling communications with a companion integrated circuit component;
> additional conductive pins for carrying additional control and communication signals;
> wherein collectively, the conductive pins of the integrated circuit component do not directly accommodate all signals lines of the system

bus, but rather directly accommodate fewer than all of the signal lines of the system bus.

The Office Action essentially copied the rejection of claim 1 and pasted it in the remarks section with respect the rejection of claim 20. In this regard, the Office Action referred to a "first logic interface" (see p. 9, line 11), even though no such element exists in claim 20.

In addition to the rejections copied from claim 1, the Office Action further concluded that "it is inherent that pins must be provided for connections between discrete chips or ICs." Finally, the Office Action alleged that "the number of total conductive pins of the integrated circuit component of Estakhri is fewer than the number of conductive pins of a corresponding conventional integrated circuit component, since split bus system is used for each IC component." In essence, the rejection of claim 20 appears to take the position that the recited features are inherent in the structure recited in claims 1 or 11, and then relies on the rejections of those claims. In response, Applicants repeat and reallege the responsive remarks (above) with respect to the inapplicability of the '906 patent to claims 1 and 11. For the same reasons, the rejection of claim 20 should be withdrawn.

As the remaining claims depend from either claim 1, 11, or 20, all remaining claims 2-10, 12-19, and 21-24 patently define over the cited art.

CONCLUSION

In view of the foregoing, it is believed that all pending claims are in proper condition for allowance. If the Examiner believes that a telephone conference would

expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

No fees are believed to be due in connection with this amendment and response. If, however, any fees are deemed to be payable, you are hereby authorized to charge any such fees to Hewlett-Packard Company's deposit account No. 08-2025.

Respectfully submitted,

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